IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT

In re application of: Hutton

Attorney Docket No.: ALTRP061/A637

Application No.: 09/783,246

Examiner: Stevens, Thomas H.

Filed: February 13, 2001

Group: 2123

Title: METHOD FOR ADAPTIVE CRITICAL PATH DELAY ESTIMATION DURING TIMING-DRIVEN PLACEMENT FOR HIERARCHICAL PROGRAMMABLE LOGIC DEVICES

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on February 23, 2006 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: _____
Joyce Ferreira

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a Notice of Appeal.

The review is requested for the reasons stated on the attached sheets.

Remarks begin on page 7 of this paper.

IN THE CLAIMS

No claim amendments are currently being made.

1. (Previously Presented) A method of estimating a critical path delay during a source electronic design placement into a target hardware device, comprising:

receiving an electronic representation of the source electronic design;

determining a path criticality in the source electronic design based on,

determining an actual delay corresponding to a connection already placed across a first boundary in the target device, and

determining a statistical estimate for a future delay corresponding to an associated future connection to be placed across a second boundary in the target device, wherein the statistical estimate for the future delay is made using estimates of future cuts not yet made in the target device; and

partitioning at least a portion of the source design by placing at least the portion of the source design across boundaries in the target device based on the determined actual delay and the statistical estimate for a future delay.

2. (Original) The method of claim 1 wherein the placing is biased towards a state in which an individual path having a relatively high criticality is not changed so as to increase an associated delay.

3. (Original) The method of claim 1 wherein the placing is biased towards a state in which an individual path having a relatively high criticality is changed in a manner that reduces the associated delay.

4. (Original) The method of claim 2 wherein the estimate for the future delay is generated by performing partitioning techniques on at least one other electronic source design.

5. (Original) The method of claim 1 wherein the electronic representation is received in the form of hardware description language coding.

6. (Original) The method of claim 1 wherein the electronic representation is received in the form of a schematic electronically captured.

7. (Original) The method of claim 1 wherein the electronic representation is received in the form selected from a group comprising: a netlist, an electronically captured schematic, and a coded hardware description language.

8. (Original) The method of claim 1 wherein the connections include at least one of conductive lines and switches.

9. (Original) The method of claim 1 wherein the target hardware device is selected from a group comprising: a complex programmable logic device (CPLD), a field programmable gate array (FPGA), an application specific integrated circuit (ASIC), a programmable logic device, a general purpose microprocessor, and a board level circuit implementation.

10. (Original) The method of claim 1 further comprising iteratively repeating the determining a path criticality and the partitioning at least a portion of the source design.

11. (Original) The method of claim 1, further comprising:

determining whether to repartition the at least a portion of the source design after the partitioning; and

if necessary, adjusting the estimates of delays from future partitions.

12. (Original) The method of claim 11 wherein determining whether to repartition at least a portion of the source electronic design is determined by comparing the critical path delays resulting from the partitioning cut with the estimate of critical path delays prior to the partitioning cut.

13. (Original) The method of claim 10 wherein adjusting the estimates of delays from future partitions comprises:

substituting a percentage of delays attributed to the partition in the statistical estimate with a new percentage derived from the critical path delay results from the partition.

14. (Previously Amended) The method of claim 1 wherein the statistical estimate for future delay comprises:

receiving at least one source design;

placing the at least one source design using partitioning methods to place the device across boundaries in the target device; and

generating statistical data corresponding to each type of boundary crossed in the target device.

15. (Original) The method of claim 14 wherein the statistical data represents the proportion of each hierarchical type of cut of the entire number of cuts in the fully placed design.

16. (Original) The method of claim 15 wherein the statistical estimates correspond to the weighted average of the statistical data generated.

17. (Original) The method of claim 16 wherein the weighted average is based on a predetermined number or percentage of the slowest delays.

18. (Original) The method of claim 16 wherein the weighted average is based on a predetermined number or percentage of the fastest delays.

19. (Previously Presented) A method for generating statistical estimates for future delays on uncut connections on a path in placing a design by partitioning methods comprising:

receiving at least one source design;

placing the at least one source design using partitioning methods to place the device across boundaries in the target device; and

generating statistical data corresponding to each type of boundary crossed in the target device, wherein the statistical data is generated using estimates of future cuts not yet made in the target device.

20. (Original) The method of claim 19 wherein the statistical data represents the proportion of each hierarchical type of cut of the entire number of cuts in the fully placed design.

21. (Original) The method of claim 19 wherein the statistical estimates correspond to the weighted average of the statistical data generated.

22. (Original) The method of claim 21 wherein the weighted average is based on a predetermined number or percentage of the slowest delays.

23. (Original) The method of claim 21 wherein the weighted average is based on a predetermined number or percentage of the fastest delays.

24. (Previously Presented) A computer program product comprising:

a machine readable memory on which is provided program instructions for a method of placing a source electronic design into a target hardware device by partitioning methods, the instructions comprising:

code for receiving an electronic representation of the source electronic design;

code for determining a path criticality in the source electronic design based on determining an actual delay corresponding to a connection already placed across a first boundary in the target device,

code for determining a statistical estimate for a future delay corresponding to an associated future connection to be placed across a second boundary associated with a future cut not yet made in the target device; and

code for partitioning at least a portion of the source design by placing the at least a portion of the source design across boundaries in the target device based on the criticalities determined.

25. (Previously Amended) The computer program product of claim 24 wherein the code for determining the statistical estimate for future delay comprises:

code for receiving at least one source design;

code for placing the at least one source design using partitioning methods to place the device across boundaries in the target device; and

code for generating statistical data corresponding to each type of boundary crossed in the target device.

26. (Original) The computer program product of claim 25 wherein the statistical data represents the proportion of each hierarchical type of cut of the entire number of cuts in the fully placed design.

27. (Original) The computer program product of claim 26 wherein the statistical estimates correspond to the weighted average of the statistical data generated.

28. (Original) The computer program product of claim 27 wherein the weighted average is based on a predetermined number or percentage of the slowest delays.

29. (Original) The computer program product of claim 28 wherein the weighted average is based on a predetermined number or percentage of the fastest delays.

30. (Previously Presented) A computer system having a central processing unit (CPU) coupled to a memory, comprising:

an interface for communicating with an individual;

wherein the computer system is configured to receive an electronic representation of the source electronic design;

wherein the computer system is further configured to,

determine a path criticality in the source electronic design based on determining an actual delay corresponding to a connection already placed across a first boundary in the target device, and

determine a statistical estimate for a future delay corresponding to an associated future connection to be placed across a second boundary associated with a future cut not yet made in the target device; and

wherein the computer system is further configured to partition at least a portion of the source design by placing the at least a portion of the source design across boundaries in the target device based on the determined actual delay.

REMARKS

Examiner Has Not Shown Teachings for Several Claim Limitations

Claims 1-30 are pending. Claims 1-30 were rejected. Claims 1-5, 8-10-12, 19, 24, and 30 including independent claims 1, 19, 24, and 30 were rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,080,201, excluding "Background of the Invention" (hereinafter referred to as Hojat A). Claims 6, 7, and 9 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hojat A and further in view of U.S. Patent No. 6,367,056 (hereinafter referred to as Lee). Claim 12 was rejected under 35 U.S.C. 103(a) as being unpatentable over Hojat A and further in view of U.S. Patent No. 6,080,201, "Background of the Invention" (hereinafter referred to as Hojat B). Claims 14-18, 20-23, and 25-29 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hojat A and further in view of U.S. Patent No. 5,237,514 (hereinafter referred to as Curtin).

The Examiner argues that Hojat A describes a synthesizer that "utilizes conventional statistical models to determine the net lengths for nets connecting objects in the same partition." The Examiner argues that the Hojat A conventional statistical model is used to "anticipate" or predict the net length for connecting objects.

The Applicants appreciate the Examiner's argument and acknowledge that Hojat A describes using conventional statistical models to model placement of nets connecting objects. "When there is more than one placeable object in a partition, each object is presumed to be in the center of the partition. In this case, the synthesizer utilizes conventional statistical models to determine the net lengths for nets connecting objects in the same partition. For objects in different partitions, the synthesizer uses conventional maze routing schemes to determine the netlengths. The maze routing scheme is preferably one which presumes no blockages, i.e., the maze router can route directly from one circuit to another without the necessity of routing around objects or changing metal layers." (Column 8: Lines 60-67)

According to various embodiments, the techniques of the present invention recognize that cuts can be made within a single partition. Hojat A's conventional statistical models do not make estimates for future delays associated with future cuts. Hojat A only presumes that each object "to be in the center of the partition" without any consideration to the fact that the partition

itself may be cut. The techniques of the present invention recognize that future cuts not yet made can significantly affect delays estimated delays. Consequently, estimates are made with consideration to future cuts not yet made.

Hojat A makes no mention of estimating future delays using estimates of future cuts not yet made. Hojat A only mentions cuts already made as partition boundaries. No mention is made of future cuts such as future cuts that can be made within a single partition. The Examiner argues that Hojat A does provide for undoing a previous cut. "In another embodiment of the invention, the placer is provided with an additional step for allowing it to undo a previous cut if the synthesizer performs an undesirable transformation." (Column 11: Lines 13-16) However, this statement actually further emphasizes that Hojat A does not teach or suggest estimating future delays using estimates of future cuts. According to various embodiments, the techniques of the present invention estimate future delays using estimates of future cuts so that future cuts not yet made do not later have to be undone. Hojat A does not consider "future cuts not yet made" and therefore has to allow "it to undo a previous cut." As noted above, a cut made in the future can significantly affect delays.

However, independent claims 1 and 19 recite "wherein the statistical estimate for the future delay is made using estimates of future cuts not yet made in the target device." Independent claims 24 and 30 recite "future delay corresponding to an associated future connection to be placed across a second boundary associated with a future cut not yet made in the target device." Independent claims 1, 19, 24, and 30 all recite "a future cut not yet made" in the target device. Hojat A makes no mention estimating delays using future cuts "not yet made." Hojat A only considers existing boundaries and existing cuts and provides that a process can undo a previous cut.

It is noted that the secondary references Hojat B, Lee, and Curtin as used along with Hojat A to reject only dependent claims. Hojat A is the only reference used to reject the independent claims. Nonetheless, Hojat B, Lee, and Curtin also fail to teach or suggest a "statistical estimate" associated with a "future cut not yet made" in the target device.

In view of the foregoing, it is respectfully submitted that the rejections of all pending claims should be withdrawn. Applicants believe that all pending claims are allowable in their

present form. Please feel free to contact the undersigned at the number provided below if there are any questions, concerns, or remaining issues.

Respectfully submitted,
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